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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHIOU-FENG CHEN, PRATEEP TUNTASOOD,
and DER-TSYR FAN

Appeal 2009-003273
Application 10/753,103
Technology Center 3600

Decided: March 3, 2010

Before JOSEPH L. DIXON, JAY P. LUCAS, and KEVIN F. TURNER, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

The Appellants appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-13, 15-22, and 24. Claims 14 and 23 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

I. STATEMENT OF THE CASE

The Invention

The invention at issue on appeal relates to a NAND flash memory and its fabrication process.

The Illustrative Claim

Claim 1, an illustrative claim, reads as follows:

> 1. A NAND flash memory cell array, comprising:
>
> a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

The References

The Examiner relies on the following references as evidence:

Chapman	US 6,118,161	Sept. 12, 2000
Sakui	US 6,411,548 B1	June 25, 2002
Hsu	US 6,911,690 B2	June 28, 2005

Brian Matas & Christian de Subercasaux, Memory 1997: Flash Memory Technology, 10-1-10-6 (1997).
Appellants' Admitted Prior Art (Fig. 1, Spec. 1) (hereafter "AAPA").

The Rejection

The following rejection is before us for review:

Claims 1-13, 15-22, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hsu and AAPA, and further in view of Chapman or Sakui.

II. ISSUE

Have Appellants shown that the Examiner erred in finding that the combination of Hsu and AAPA, with Chapman, or Sakui, teaches or fairly suggests "a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region" and "the last select gate in the row at least partially overlapping the source region," as recited in independent claim 1?

III. PRINCIPLES OF LAW

Prima Facie Case of Unpatentability

Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Obviousness

"Obviousness is a question of law based on underlying findings of fact." *In re Kubin*, 561 F.3d 1351, 1355 (Fed. Cir. 2009). The underlying factual inquiries are: (1) the scope and content of the prior art, (2) the differences between the prior art and the claims at issue, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations of

nonobviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citation omitted).

IV. FINDINGS OF FACT

The following findings of fact (FFs) are supported by a preponderance of the evidence.

AAPA

1. In Fig. 1, the Appellants disclose an element 22 as a bit line diffusion (bit line), and an element 32 as a bit line contact (Spec. 2, ll. 1-2) and the select gate 31 partially overlaps the source region 23 (Spec. 2, ll. 8-9).

Hsu

2. Hsu discloses a NAND flash memory structure that has no diffusion areas between source 126 and drain 124 (Figs. 1A and 1C; col. 6 ll. 6-7), and the drain region 124 is the bit line (diffusion) (col. 8, l. 55).

3. Hsu also discloses that the fabrication process of select gates and the stacked gates, i.e., floating gates and control gates, repeatedly utilizes a chemical vapor deposition (CVD) process, and a photolithography etching process (col. 7, l. 23-col. 8, l. 31; Figs. 2D-2F). The stacked gates and the selected gates are, thus, formed on the substrate based on the patterned photo masks, which are aligned with each other (col. 7. l. 15-col. 8 l. 1; Figs. 2D-2F). Therefore, the stacked gates and select gates are self-aligned.

4. Hsu further discloses that a tunneling layer 116 has the thickness 60-90 Å, the inner gate layer 122 has the thickness 70/70/60 Å,

and a spacer 114 which is thicker than the tunneling layer 116 (Fig. 1B and 1C; col. 5, ll. 23-57).

5. Hsu further discloses that the structure of the NAND flash memory would reduce the working voltage, and thereby enhance the NAND flash memory's speed and efficiency (col. 6, ll. 28-42), and the structure of the NAND flash memory has the control gates 120 and the select gates 110 surround the floating gates 180 (Fig. 1B; col. 5, ll. 4-6).

6. Hsu further discloses that during the erasing operation, the erase path is from the floating gates extended to the substrate, a 11V is applied to source region, and a 0V is applied to select gates and control gates to push the electrons from the floating gates to the substrate for erasing (Fig. 3; col. 8, ll. 63-67).

7. Hsu further discloses a NAND flash memory that:

> [b]efore programming the array, *a 4.5V, a 7V, a 11V, and a 0V are applied to the source region, SG1-SG4, CG1-CG4, and the drain region respectively*, to turn on the channels of Qn1-Qn4. During programming the array, using *Qn2 as an example, a 4.5V, a 1.5V, a 7V, a 9V, a 11V, and a 0V are applied to the source region, the selected select gate line SG2, the non-selected select gate lines (SG1, SG3, and SG4), the selected control gate line CG2, the non-selected control gate lines (CG1, CG3, and CG4), and the substrate respectively*, to cause source-side injection in order to inject electrons into the selected flash memory cell Qn2 and program it.

(Col. 8, ll. 41-52 (emphasis added); *see also* Fig. 3).

8. Hsu further discloses that:

> [d]uring reading the data from the array, *a 0V, a 4.5V, a 1.5V, and a 1.5V are applied to the source region, SG1-SG4, CG1-CG4, and the drain region (the bit line)* respectively. The value of the cell ("0" of "1") depends on whether the floating gate is *negatively charged* or positively charged. If the floating gate is negatively charged, the flash memory cell's channel is off and the current is small. On the other hand, if the floating gate is positively charged, the flash memory cell's channel is on and the current can pass through the channel.

(Col. 8, ll. 53-62 (emphasis added); *see also* Fig. 3).

Sakui

9. Sakui discloses that a select gate line 27 (GSL) partially overlaps the source region 28s (Figs. 30-31; col. 30, ll. 14-42).

10. Sakui further discloses that an erase pulse could be sufficient at -3V and different erase voltages may be applied (col. 23, ll. 17-25, Table I).

V. ANALYSIS

The Examiner sets forth a detailed explanation of a reasoned conclusion of unpatentability in the Examiner's Answer. Therefore, we look to Appellants' Briefs to show error therein. *See In re Kahn*, 441 F.3d at 985-86.

Grouping of Claims

The Appellants have elected to argue claims 1-13 together as a group (App. Br. 6). Therefore, we select independent claim 1 as the representative claim for this group, and we will address the Appellants' arguments with respect thereto. 37 C.F.R. § 41.37 (c)(1)(vii). *See In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987). For completeness, we will

also briefly address the Appellants' contentions as to dependent claims 2-13.

35 U.S.C. § 103(a) rejections

With respect to claim 1, the Appellants contend that claim 1 is allowable because the Examiner failed to provide any support for characterizing the drain region 124 as a bit line diffusion (App. Br. 5-6; Reply Br. 2). The Appellants further contend that "the Examiner also makes the illogical, unsupported and totally specious argument that a bit line diffusion inherently is contacted with a bit line and that both a bit line and a bit line contact must therefore exist." (App. Br. 5.)

We disagree with the Appellants' contentions. We agree with the claim construction of the Examiner that the bit line diffusion is a diffusion region for a bit line (Ans. 4).

We find that AAPA clearly teaches a bit line diffusion, bit line contact, and bit line with NAND flash memory (FF 1). We also find that Hsu expressly mentions that the drain region 124 is the bit line (diffusion), and that there are no other diffusions between the drain and the source regions (FF 2). We, therefore, conclude that combining the well-known elements of bit line and bit line contact of NAND flash memory in AAPA with the bit line diffusion of Hsu and the well-known technique of no other diffusions between the source and drain regions taught by Hsu is nothing more than the "predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 417.

The Appellants further contend that "neither Sakui et al. nor the prior art discussed in the background section of applicant's disclosure even

remotely suggests a select gate which partially overlaps a source region in a memory cell array" (App. Br. 5), and adding a select gate or removing a memory cell to achieve the claimed structure would be "far beyond the teaching of the references." (Reply Br. 2.)

We disagree with the Appellants' contentions. We find that AAPA clearly shows that the select gate 31 partially overlaps the source gate 23 (FF 1). We also find that Sakui teaches that a select gate line 27 (GSL) partially overlaps the source region 28s (FF 8).

The Supreme Court noted that an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. Furthermore, one of ordinary skill in the art is also a person of ordinary creativity, not an automaton. *Id.* at 421. The structure of a NAND flash memory that partially overlaps a select gate on a source region is a desirable way to create lower capacitance and would have been within the skill in the art, as evidenced by AAPA and Sakui. One of ordinary skill in the art would recognize that AAPA's or Sakui's method would improve the similar memory cell of Hsu in the same or similar way. We find that the combination of either AAPA or Sakui and Hsu is "a design step well within the grasp of a person of ordinary skill in the relevant art" and the benefit of doing so would be obvious. *Id.* at 427.

The Appellants have not shown that employing the technique of partially overlapping a select gate on a source region in Hsu was uniquely challenging or difficult for one of ordinary skill in the art or represented an unobvious step over the prior art. Accordingly, we sustain the Examiner's

obviousness rejection of claim 1.

With respect claim 2, the Appellants further contend that "[t]here is no support whatsoever for the statement that stacked gates and select gates are aligned to each other." (App. Br. 6.)

We disagree with the Appellants' contention. We find that Hsu fabricates the stacked gates and select gates utilizing CVD, followed by an ion implantation, and a photolithography etching process which is similar to the instant invention (FF 3), and thus, the stacked gates and select gates are aligned to each other.

With respect claim 3, the Appellants further contend that "Hsu et al. is silent as to the relative thickness of the different dielectrics." (App. Br. 6.)

We disagree with the Appellants' contention. We find that Hsu teaches that the tunneling layer is the thinnest layer among the three layers (FF 4).

With respect claim 4, the Appellants further contend that "the Examiner has failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates." (App. Br. 7.)

We disagree with the Appellants' contention. We find that Hsu teaches that the control gates and the select gates surround the floating gates (FF 5).

With respect to claim 5, the Appellants further contend that the Examiner provides no support for the rejection of the claimed limitation (App. Br. 7).

We disagree with the Appellants' contention. We find Hsu teaches that the erase path extends from the floating gates through the thin tunnel

layer to the substrate with the voltage coupled to floating gates from the surrounding control gates and the select gates (FF 5 and FF 6).

With respect to claims 6 and 7, the Appellants further contend that the Examiner provides no support for the rejection of the claimed limitation (App. Br. 7).

We disagree with the Appellants' contention. We find that Hsu teaches that the programming path extends to the select gate SG2 and the floating gate to floating gate because the floating gate is positively charged (the source is at 4.5V, the selected gate SG2 is at 1.5V, other non-selected gates SG1, SG3, and SG4 are at 7V, the selected CG2 is at 9V, and the substrate is at 0V) to cause the source-side injection for the selected memory cell (FF 7).

With respect to claim 8, the Appellants further contend that the Examiner provides no support for the rejection of the claimed limitation and only argued the intended use for the structure limitation (App. Br. 8).

We disagree with the Appellants' contention. We find that Hsu teaches that the select gates in unselected cells are biased at a voltage that positively charged the floating gate adjacent to the select gates, and then a conduction path formed between the bit line diffusion (drain) and the source region (FF 7 and FF 8).

With respect to claim 9, the Appellants further contend that the Examiner provides no support for the rejection of the claimed limitation (App. Br. 8).

We disagree with the Appellants' contention. We find that Hsu teaches that the source is at 4.5V, the selected gate SG2 is at 1.5V, other

non-selected gates SG1, SG3, and SG4 are at 7V, the selected CG2 is at 9V, and the non-selected gate CG1, CG3, and CG4 are at 11V (FF 7).

With respect to claims 10-13, the Appellants further contend that the Examiner provides no support for the rejection of the claimed limitation and only argued the intended use for the claimed structure (App. Br. 8-9).

We disagree with the Appellants' contention. We find that Hsu teaches that 0V is applied to the source, SG1-SG4, and CG1-CG4, and the erase pulse 11V is applied to the substrate to erase the data in the cell array (FF 6). Sakui teaches that different negative voltages could be applied for erasing operation (FF 10).

Accordingly, we sustain the Examiner's obviousness rejection of claims 2-13.

With respect to claims 15 and 19, the Appellants set forth similar arguments as those presented with respect to of claim 1. Since we sustain the Examiner's rejection of claim 1, we also sustain the obviousness rejection of claims 15 and 19.

With respect to claims 16-18 and 20-22, the Appellants set forth similar arguments as those presented with respect to claims 2-4. Since we sustain the Examiner's rejection of claims 2-4, we also sustain the obviousness rejection of claims 16-18 and 20-22.

With respect to claim 24, the Appellants contend that combination of references not only fails to teach or fairly suggest the bit line diffusion and no other diffusion areas between the source and the bit line diffusion, but

also fails to teach or fairly suggest the "self-aligned" and "the voltage coupling from the control gates and the select gates to the floating gates" limitations (App. Br. 11).

We disagree with the Appellants' contentions. As discussed above, we find that Hsu teaches the limitation of the bit line diffusion and no other diffusion areas between the source and the bit line diffusion (FF 1 and FF 2). As to "self-aligned" limitation, as discussed with respect to claim 2, we find that the limitation is taught by Hsu (FF 3). As to the limitation of "the voltage coupling from the control gates and the select gates to the floating gates," we find that Hsu teaches that the voltage is coupled from the control gates and the select gates to the floating gates for reading operation (FF 8).

Accordingly, we sustain the Examiner's obviousness rejection of claim 24.

VI. CONCLUSION

Based on our consideration of the totality of the record before us, we have weighed the evidence of obviousness found in the combined teachings of the applied references, with Appellants' countervailing evidence and arguments for nonobviousness and conclude that the claimed invention encompassed by appealed claims 1-13, 15-22, and 24 would have been obvious as a matter of law under 35 U.S.C. § 103(a).

VII. DECISION

We affirm the obviousness rejections of claims 1-13, 15-22, and 24 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with

this appeal may be extended under 37 C.F.R. § 1.136 (a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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